18GHz Microwave PLL Synthesizer

Preliminary Technical Data

ADF41020

FEATURES

18 GHz maximum RF input frequency
Integrated SiGe prescaler
Software compatible with popular ADF410x family of PLLs
2.7 V to 3.3 V PLL power supply
Programmable dual-modulus prescaler
8/9, 16/17, 32/33, 64/65
Programmable charge pump currents
3-wire serial interface
Analog and digital lock detect
Hardware and software power-down mode

APPLICATIONS

Microwave Point to Point / Multi-Point Radios
Wireless infrastructure
VSAT Radios
Test equipment
Instrumentation

GENERAL DESCRIPTION

The ADF41020 frequency synthesizer can be used to implement local oscillators as high as 18 GHz in the up-conversion and down-conversion sections of wireless receivers and transmitters. It consists of a low noise, digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider and high frequency programmable feedback dividers (A,B & P). A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). The synthesizer can be used to drive external microwave VCOs via an active loop filter. Its very high bandwidth means a frequency doubler stage can be eliminated, simplifying system architecture and reducing cost. The ADF41020 is software compatible with the existing ADF4106/7/8 family of devices from Analog Devices. The pin-out matches very closely with the exception of the single-ended RF input pin, meaning only a minor layout change is required when updating your design.

FUNCTIONAL BLOCK DIAGRAM

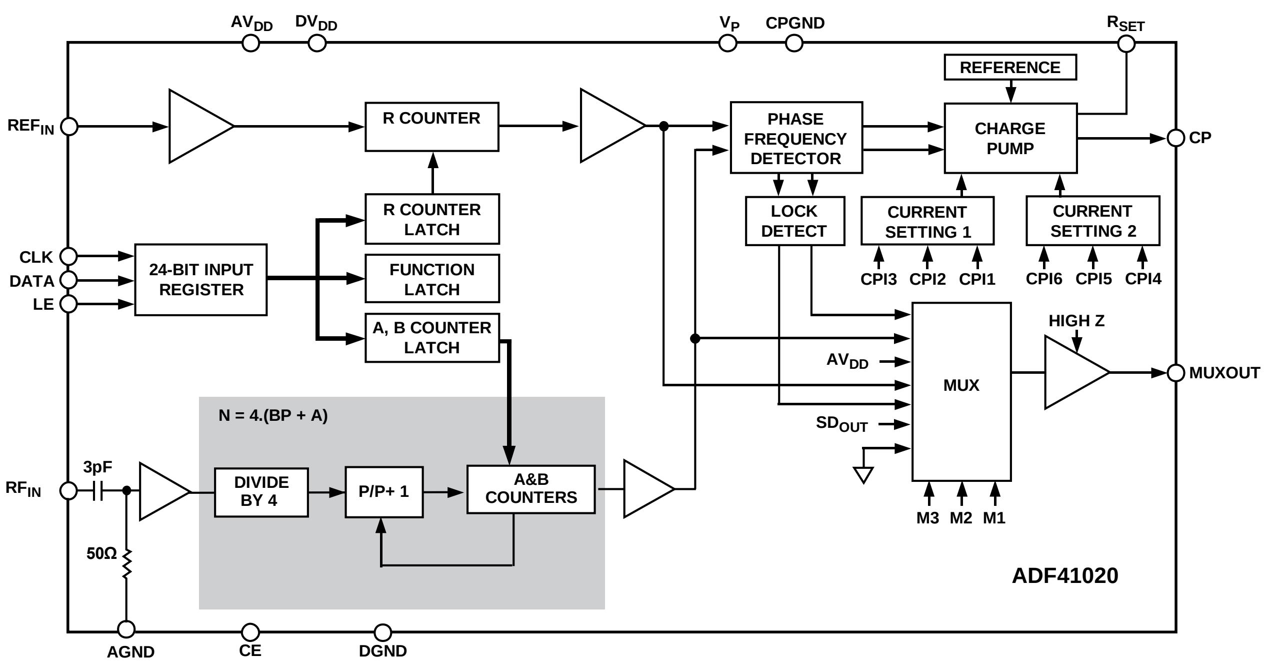

Figure 1.

Rev. PrE

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REVISION HISTORY

SPECIFICATIONS

DV_{DD} = AV_{DD} = 3 V ± 10%, V_P = 3 V, GND = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Conditions/Comments
RF CHARACTERISTICS					See Figure 10 for input circuit.
RF Input Frequency (RF_{IN})	4.0		18.0	GHz	
RF Input Sensitivity	−10		+10	dBm	
Maximum Allowable Prescaler Output Frequency[1]			TBD	MHz	P=8
			TBD	MHz	P=16
REF_{IN} CHARACTERISTICS					
REF_{IN} Input Frequency	TBD		TBD	MHz	
REF_{IN} Input Sensitivity	TBD		TBD	V p-p	Biased at DV_{DD} / 2 when input is ac-coupled
REF_{IN} Input Capacitance			10	pF	
REF_{IN} Input Current			±100	µA	
PHASE DETECTOR					
Phase Detector Frequency[2]			104	MHz	
CHARGE PUMP					Programmable, see Table 8
I_{CP} Sink/Source					
High Value		5.0		mA	With R_{SET} = 5.1 kΩ
Low Value		625		µA	
Absolute Accuracy		2.5		%	With R_{SET} = 5.1 kΩ
R_{SET} Range	5.1	5.1	11	kΩ	See Table 8
I_{CP} Three-State Leakage		1	2 nA	nA	T_A = 25°C
Sink and Source Current Matching		2		%	0.5 V ≤ V_{CP} ≤ V_P – 0.5 V
I_{CP} vs. V_{CP}		1.5		%	0.5 V ≤ V_{CP} ≤ V_P – 0.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = V_P/2
LOGIC INPUTS					
V_{IH}, Input High Voltage	1.4			V	The SPI interface is 1.8V & 3V logic compatible
V_{IL}, Input Low Voltage			0.6	V	
I_{INH}, I_{INL}, Input Current			±1	µA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	1.4			V	Open-drain output chosen, 1 kΩ pull-up resistor to 1.8 V
V_{OH}, Output High Voltage	DV_{DD} - 0.4			V	CMOS output chosen
I_{OH}			500	µA	
V_{OL}, Output Low Voltage			0.4	V	
I_{OL}			500	µA	
POWER SUPPLIES					
AV_{DD}	2.7		3.3	V	
DV_{DD}	2.7		3.3	V	
V_P	2.7		3.3	V	
I_{DD}[3]		30	TBD	mA	
I_P		0.8	TBD	mA	T_A = 25°C
Power-Down Mode		TBD		µA	

Parameter	Min	Typ	Max	Unit	Conditions/Comments
NOISE CHARACTERISTICS					
ADF41020 Normalized Phase Noise Floor[4]		– 222		dBc/Hz	PLL Loop BW = 500kHz
ADF41020 Normalized 1/f Noise		– 118		dBc/Hz	Measured at 10kHz offset. Normalized to 1GHz
Phase Noise Performance[5]					@ VCO output
6 GHz		– TBD		dBc/Hz	@ 10 kHz offset and 1 MHz PFD frequency
12 GHz		– TBD		dBc/Hz	@ 10 kHz offset and 1 MHz PFD frequency
18 GHz		– TBD		dBc/Hz	@ 10 kHz offset and 1 MHz PFD frequency
Spurious Signals					
6 GHz		– TBD		dBc	@ 1 MHz/2 MHz and 1 MHz PFD frequency
12 GHz		– TBD		dBc	@ 1 MHz/2 MHz and 1 MHz PFD frequency
18GHz		– TBD		dBc	@ 1 MHz/2 MHz and 1 MHz PFD frequency

[1] This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[2] Guaranteed by design. Sample tested to ensure compliance.
[3] T_A = 25°C; V_{DD} = 3 V; P = 32; RF_{IN} = 12.0 GHz.
[4] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log N (where N is the N divider value) and 10 log F_{PFD}. $PN_{SYNTH} = PN_{TOT} - 10 \log F_{PFD} - 20 \log N$.
[5] The phase noise is measured with the EVAL-ADF41013EB1 evaluation board and the Rhode&Schwarz FSUP Spectrum Analyzer. The reference is provided by a Rhode&Schwarz SMA100A.

TIMING CHARACTERISITICS

$AV_{DD} = DV_{DD} = 3$ V, $V_P = 3$ V, GND = 0 V, $R_{SET} = 5.1$ kΩ, dBm referred to 50 Ω, $T_A = T_{MAX}$ to T_{MIN}, unless otherwise noted.

Table 1.

Parameter	Limit	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Setup Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Setup Time
t_6	20	ns min	LE Pulse Width

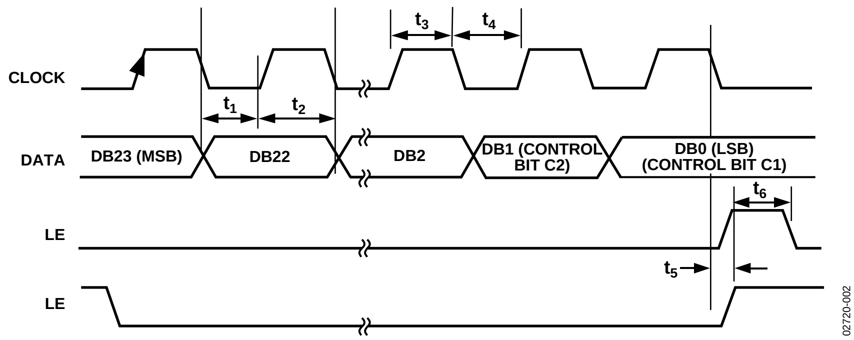

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
AV_{DD} to GND	−0.3 V to + 3.6 V
AV_{DD} to DV_{DD}	−0.3 V to + 0.3 V
V_P to GND	−0.3 V to + 3.6 V
V_P to AV_{DD}	−0.3 V to + 0.3 V
Digital I/O Voltage, REF_{IN} to GND	−0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_P + 0.3 V
REF_{IN}, RF_{IN} to GND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	TBD °C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Transistor Count	
CMOS	Tbd
Bipolar	Tbd

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

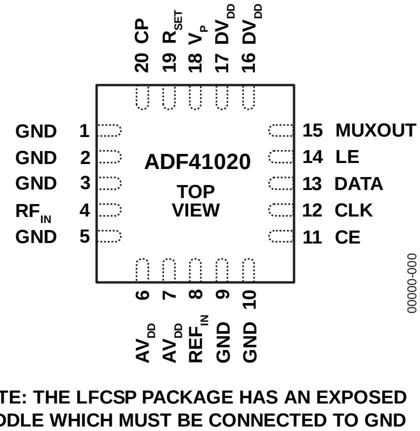

Figure 3. 20-Lead LFCSP_VQ Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1,2,3,5,9,10	GND	Ground Pins..
4	RF_{IN}	Input to the RF Prescaler. This input is ac-coupled internally.
6, 7	AV_{DD}	Analog Power Supply. This may range from 2.7 V to 3.3 V. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. Pin 6 is the supply for the fixed divide-by-4 prescaler.
8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $DV_{DD}/2$ and a dc equivalent input resistance of 100 kΩ. See Figure 9. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device, depending on the status of the power-down bit, PD1.
12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches with the latch being selected using the control bits.
15	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
16, 17	DV_{DD}	Digital Power Supply. This may range from 2.7 V to 3.3 V. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
18	V_P	Charge Pump Power Supply.
19	R_{SET}	Connecting a resistor between this pin and GND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $$I_{CP\,MAX} = \frac{25.5}{R_{SET}}$$ So, with R_{SET} = 5.1 kΩ, $I_{CP\,MAX}$ = 5.0 mA.
20	CP	Charge Pump Output. When enabled, this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

Figure 4

TBD

Figure 5

TBD

Figure 6

TBD

Figure 7

TBD

Figure 8

GENERAL DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 9. SW1 and SW2 are normally closed switches. SW3 is a normally open switch. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

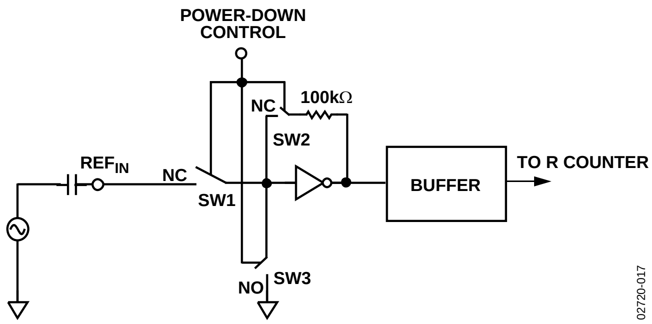

Figure 9. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 10. It is followed by a buffer which generates the differential CML levels needed for the prescaler.

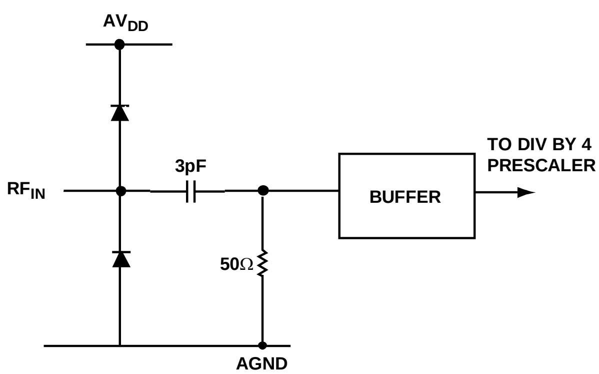

Figure 10. RF Input Stage

PRESCALER

The ADF41020 uses a two prescaler approach to achieve operation up to 18GHz. The first prescaler, is a fixed divide-by-4 block. The second prescaler which takes its input from the divide-by-4 output is implemented as a dual-modulus prescaler (P/P + 1) which allows finer frequency resolution versus a fixed prescaler. Along with the A counter and B counter, this enables the large division ratio, N, to be realized (N = 4(BP + A)). The dual-modulus prescaler, operating at CML levels, takes the clock from the fixed prescaler stage and divides it down to a manageable frequency for the CMOS A counter and B counters. The second prescaler is programmable. It can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core. There is a minimum divide ratio possible for fully contiguous output frequencies. This minimum is given by $4(P^2 – P)$.

A COUNTER AND B COUNTER

The A counter and B counter combine with the two prescalers to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is TBD MHz or less.

Pulse Swallow Function

Because of the fixed divide-by-4 block, the generated output frequencies are spaced by four times the reference frequency divided by R. The equation for the VCO frequency is

$$f_{VCO} = [(P \times B) + A] \times \frac{4.f_{REFIN}}{R}$$

where:

f_{VCO} is the output frequency of the external voltage controlled oscillator (VCO).

P is the preset modulus of the dual-modulus prescaler (8/9, 16/17, etc.).

B is the preset divide ratio of the binary 13-bit counter (3 to 8191).

A is the preset divide ratio of the binary 6-bit swallow counter (0 to 63).

f_{REFIN} is the external reference frequency oscillator.

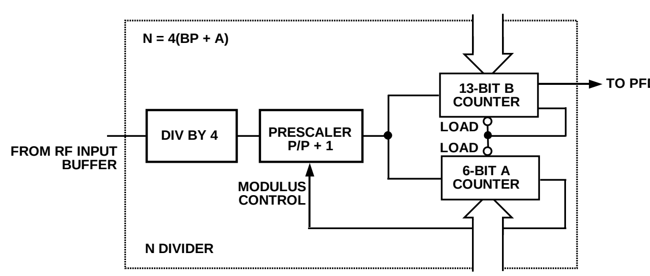

Figure 11. Prescalers, A and B Counters that make up the N-Divide value

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 12 is a simplified schematic. The PFD includes a fixed delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. The charge pump converts the PFD output to current pulses, which are integrated by the PLL loop filter.

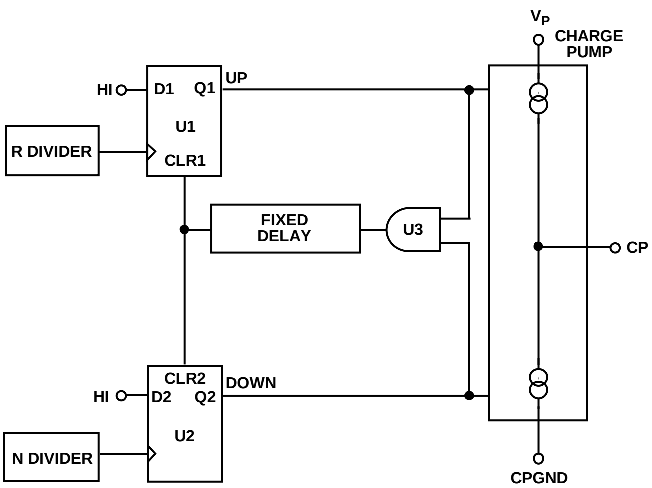

Figure 12. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF41020 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Table 8 shows the full truth table. Figure 13 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

The N-channel, open-drain, analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock is detected, this output is high with narrow, low-going pulses.

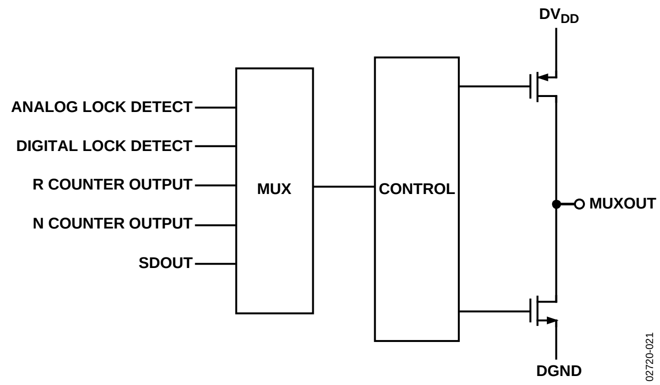

Figure 13. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF41020 digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram of Figure 2. The truth table for these bits is shown in Table 4. Table 5 shows a summary of how the latches are programmed. The SPI is both 1.8V & 3V compatible.

Table 4. C1, C2 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	R Counter
0	1	N Counter (A and B)
1	0	Function Latch (Including Prescaler)

Table 5. Latch Summary

REFERENCE COUNTER LATCH

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

FUNCTION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

Table 6. Reference Counter Latch Map

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LOL1	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

R14	R13	R12	....	R3	R2	R1	DIVIDE RATIO
0	0	0	....	0	0	1	1
0	0	0	....	0	1	0	2
0	0	0	....	0	1	1	3
0	0	0	....	1	0	0	4
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
1	1	1	....	1	0	0	16380
1	1	1	....	1	0	1	16381
1	1	1	....	1	1	0	16382
1	1	1	....	1	1	1	16383

ABP2	ABP1	ANTIBACKLASH PULSE WIDTH
0	0	2.9ns
0	1	1.3ns
1	0	6.0ns
1	1	2.9ns

TEST MODE BITS SHOULD BE SET TO 00 FOR NORMAL OPERATION.

LDP	OPERATION
0	THREE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.
1	FIVE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.

BOTH OF THESE BITS MUST BE SET TO 0 FOR NORMAL OPERATION.

LOL1	Loss of Lock
0	Loss of Lock Enable
1	Loss of Lock Disable

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Table 7. N (A, B) Counter Latch Map

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

X = DON'T CARE

A6	A5	....	A2	A1	A COUNTER DIVIDE RATIO
0	0	....	0	0	0
0	0	....	0	1	1
0	0	....	1	0	2
0	0	....	1	1	3
.	.	....	.	.	.
.	.	....	.	.	.
.	.	....	.	.	.
1	1	....	0	0	60
1	1	....	0	1	61
1	1	....	1	0	62
1	1	....	1	1	63

B13	B12	B11		B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	....	0	0	0	NOT ALLOWED
0	0	0	....	0	0	1	NOT ALLOWED
0	0	0	....	0	1	0	NOT ALLOWED
0	0	0	....	0	1	1	3
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
.	.	.	....	.	.	.	.
1	1	1	....	1	0	0	8188
1	1	1	....	1	0	1	8189
1	1	1	....	1	1	0	8190
1	1	1	....	1	1	1	8191

F4 (FUNCTION LATCH) FASTLOCK ENABLE	CP GAIN	OPERATION
0	0	CHARGE PUMP CURRENT SETTING 1 IS PERMANENTLY USED.
0	1	CHARGE PUMP CURRENT SETTING 2 IS PERMANENTLY USED.
1	0	CHARGE PUMP CURRENT SETTING 1 IS USED.
1	1	CHARGE PUMP CURRENT IS SWITCHED TO SETTING 2. THE TIME SPENT IN SETTING 2 IS DEPENDENT ON WHICH FASTLOCK MODE IS USED. SEE FUNCTION LATCH DESCRIPTION.

N = 4(BP + A), P IS PRESCALER VALUE SET IN THE FUNCTION LATCH. B MUST BE GREATER THAN OR EQUAL TO A. FOR CONTINUOUSLY ADJACENT VALUES OF ($N \times F_{REF}$), AT THE OUTPUT, N_{MIN} IS $4(P^2 - P)$.

THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS.

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Table 8. Function Latch Map

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	N-CHANNEL OPEN-DRAIN LOCK DETECT
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

CPI6	CPI5	CPI4	I_{CP} (mA)	
CPI3	CPI2	CPI1	5.1kΩ	11kΩ
0	0	0	0.625	0.289
0	0	1	1.25	0.580
0	1	0	1.875	0.870
0	1	1	2.5	1.160
1	0	0	3.125	1.450
1	0	1	3.75	1.730
1	1	0	4.375	2.020
1	1	1	5.0	2.320

CE PIN	PD2	PD1	MODE
0	0	X	ASYNCHRONOUS POWER-DOWN
1	0	0	NORMAL OPERATION
1	0	1	SOFTWARE POWER-DOWN

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

02720-025

THE FUNCTION LATCH

With C2 and C1 set to 1 and 0, respectively, the on-chip function latch is programmed. Table 8 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this is 1, the R counter and the N (A, B) counter are reset. For normal operation, this bit should be 0. When powering up, disable the F1 bit (set to 0). The N counter will then resume counting in close alignment with the R counter. (The maximum error is one prescaler cycle).

Power-Down

Bit DB3 (PD1) provides a software power-down mode to reduce the overall current drawn by the device. It is enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the state of PD1.

In the programmed software power-down, the device powers down immediately after latching 1 into the PD1 bit. PD2 is a reserved bit and should be cleared to 0.

When a power-down is activated, the following events occur:

- All active dc current paths in the main synthesizer section are removed. The RF divide-by-4 prescaler remains active however.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital clock detect circuitry is reset.
- The RF_{IN} input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF41020 family. Table 8 shows the truth table.

Fastlock Enable Bit

DB9 of the function latch is the fastlock enable bit. When this bit is 1, fastlock is enabled.

Fastlock Mode Bit

DB10 of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, then Fastlock Mode 1 is selected; and if the fastlock mode bit is 1, then Fastlock Mode 2 is selected.

Fastlock Mode 1

The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock when 1 is written to the CP gain bit in the N (A, B) counter latch. The device exits fastlock when 0 is written to the CP gain bit in the N (A, B) counter latch.

Fastlock Mode 2

The charge pump current is switched to the contents of Current Setting 2. The device enters fastlock when 1 is written to the CP gain bit in the N (A, B) counter latch. The device exits fastlock under the control of the timer counter. After the timeout period, which is determined by the value in TC4 to TC1, the CP gain bit in the N (A, B) counter latch is automatically reset to 0, and the device reverts to normal mode instead of fastlock. See Table 8 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is that Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is used when the system is dynamic and in a state of change (that is, when a new output frequency is programmed). The normal sequence of events follows.

The user initially decides what the preferred charge pump currents are going to be. For example, the choice may be 0.85 mA as Current Setting 1 and 1.7 mA as the Current Setting 2.

Simultaneously, the decision must be made as to how long the secondary current stays active before reverting to the primary current. This is controlled by the timer counter control bits, DB14 to DB11 (TC4 to TC1), in the function latch. The truth table is given in Table 8.

To program a new output frequency, simply program the N (A, B) counter latch with new values for A and B. Simultaneously, the CP gain bit can be set to 1, which sets the charge pump with the value in CPI6 to CPI4 for a period of time determined by TC4 to TC1. When this time is up, the charge pump current reverts to the value set by CPI3 to CPI1. At the same time, the CP gain bit in the N (A, B) counter latch is reset to 0 and is now ready for the next time the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.

Charge Pump Currents

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. The truth table is given in Table 8.

Prescaler Value

P2 and P1 in the function latch set the programmable P prescaler value. The P value should be chosen so that the prescaler output frequency is always less than or equal to TBD MHz.

PD Polarity

This bit sets the phase detector polarity bit. See Table 8.

CP Three-State

This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

Device Programming After Initial Power-Up

After initial power up of the device, there are three methods for programming the device: function latch, CE pin, and counter reset.

Function Latch Method

- Apply V_{DD}.
- Program the function latch load (10 in two LSBs of the control word), making sure that the F1 bit is programmed to a 0.
- Do an R load (00 in two LSBs).
- Do an N (A, B) load (01 in two LSBs).

CE PIN METHOD

- Apply V_{DD}.
- Bring CE low to put the device into power-down. This is an asychronous power-down in that it happens immediately.
- Program the function latch (10).
- Program the R counter latch (00).
- Program the N (A, B) counter latch (01).
- Bring CE high to take the device out of power-down. The R and N (A, B) counters now resume counting in close alignment.

Note that after CE goes high, a 1 µs duration may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it is programmed at least once after V_{DD} is initially applied.

COUNTER RESET METHOD

- Apply V_{DD}.
- Do a function latch load (10 in two LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
- Do an R counter load (00 in two LSBs).
- Do an N (A, B) counter load (01 in two LSBs).
- Do a function latch load (10 in two LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides offers direct control over the internal counter reset.

APPLICATIONS

INTERFACING

The ADF41020 has a simple 1.8V & 3V SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE goes high, the 24 bits clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 4 for the latch truth table.

The maximum allowable serial clock rate is TBD MHz.

ADuC7020 Interface

Figure 14 shows the interface between the ADF41020 and the ADuC70xx family of analog microcontrollers. The ADuC70xx family is based on an AMR7 core, although the same interface can be used with any 8051-based microcontroller. The microcontroller is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF41020 needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the microcontroller to the device. When the third byte is written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF41020, it needs three writes (one each to the function latch, R counter latch, and N counter latch) for the output to become active.

I/O port lines on the microcontroller are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SPI transfer rate of the ADuC7023 is 20Mbps. This means that the maximum rate at which the output frequency can be changed is 833 kHz. If using a faster SPI clock just make sure the SPI timing requirements listed in Table 1 are adhered to.

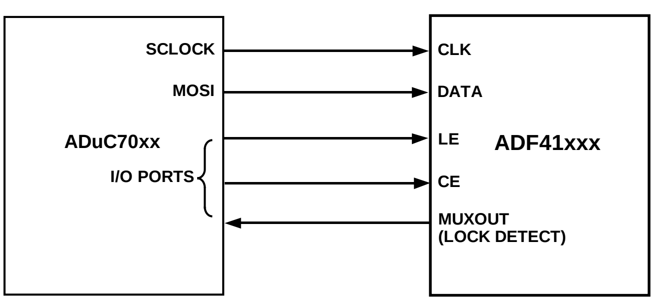

Figure 14. ADuC7020-to-ADF41020 Interface

Blackfin BF527 Interface

Figure 15 shows the interface between the ADF41020 and the Blackfin ADSP-BF527 digital signal processor (DSP). The ADF41020 needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the Blackfin family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer. As in the microcontroller case just make sure the clock speeds are within the maximum limits outlined in table 1.

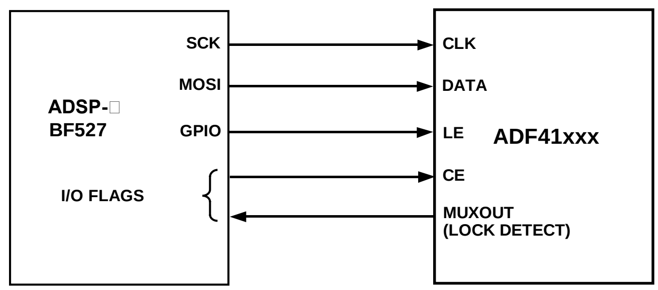

Figure 15.ADSP-BF527-to-ADF41020 Interface

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the LFCSP (CP-20) are rectangular. The printed circuit board (PCB) pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the LFCSP has a central thermal pad.

The thermal pad on the PCB should be at least as large as this exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias may be used on the PCB thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

The user should connect the PCB thermal pad to GND.

OUTLINE DIMENSIONS

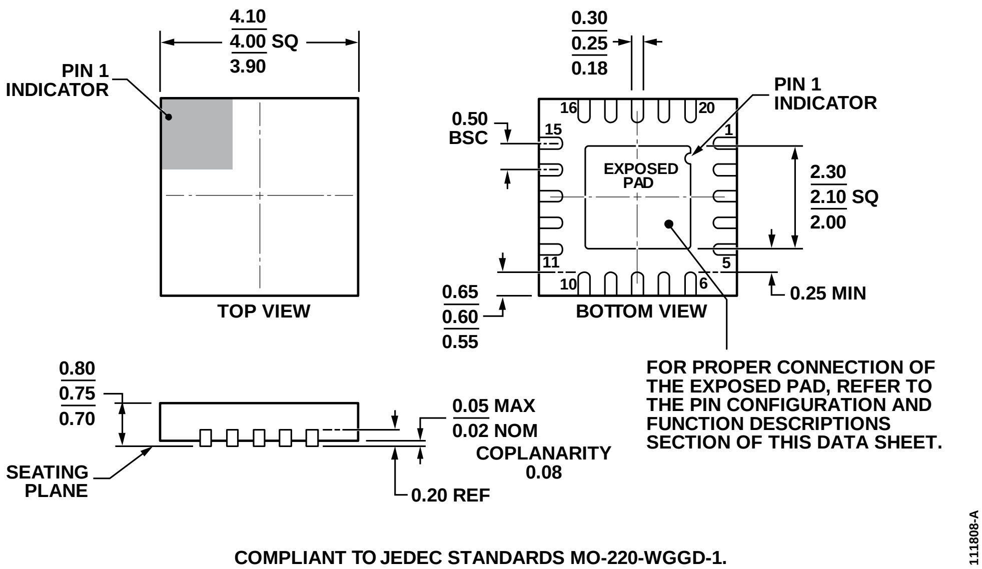

Figure 16. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-20-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF41020BCPZ-U1	–40°C to + 85°C	20-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-20-6
EVAL-ADF41020EB1Z-U1		Evaluation Board	

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